REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Final Office Action dated 24 March 2008. Responsive to the rejections made in the Official Action, Claims 1, 14, and 16 have been amended to clarify the combination of elements that establishes the inventive concept presented in the subject Patent Application.

In the Official Action, the Examiner rejected Claims 1-3 and 14 under 35 U.S.C. § 103(a), as being unpatentable over Rofougaran, et al., U.S. Patent Application Publication 2008/0045162, in view of Prockup, U.S. Patent 6,760,571, and further in view of Ishigaki, U.S. Patent 5,832,027. Claims 4-7 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Rofougaran, et al. in view of Prockup and Ishigaki, and further in view of Tian, U.S. Patent 6,624,710. Claim 11 was rejected under 35 U.S.C. § 103(a), as being unpatentable over Rofougaran, et al. in view of Prockup and Ishigaki, and further in view of Yamazaki, et al., U.S. Patent 5,398,007. Still further, Claims 8-10 and 19-22 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Rofougaran, et al. in view of Prockup and Ishigaki, and Tian, and further in view of Yamazaki, et al. In addition, Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rofougaran, et al. in view of Ishigaki and further in view of Tian.

Before discussing the prior art relied upon by the Examiner, it is believed beneficial to first briefly review the structure and method of the invention of the subject Patent Application, as now claimed. The invention of the subject Patent Application is directed to an RF transmitter system which includes a microprocessor having a control signal output and a data output for output of digital data to be transmitted, and a converter coupled to the microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system.

The system includes an external crystal oscillator and a local oscillator which receives a signal from the external crystal oscillator and, in response thereto, generates a first clock signal having a frequency in a radio frequency band. A clock switch is provided that is coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter. The third clock signal is different in frequency from the first clock signal and the second clock signal. The clock switch has an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal.

The RF transmitter system further includes a transmitter connected to an output of the converter for receiving the digital packet data and is coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital

packet data to be transmitted by the transmitter. The microprocessor, converter, local oscillator, clock switch and transmitter are integrated on a single chip. Thus, the microprocessor provides commands for controlling the operation of the RF transmitter system operation and provides the digital data output that is converted into digital packet data for transmission.

The present invention is also directed to a method for transmitting data with an RF transmitter system which includes a microprocessor connected with a converter that is in turn connected to a transmitter. The method includes the step of receiving, at the local oscillator, a frequency signal from an external crystal oscillator and generating, at the local oscillator, a first clock signal at a radio frequency in response to the external crystal oscillator frequency signal upon receipt of a control signal from the microprocessor to start generation of the first clock signal. The first clock signal is coupled to the transmitter. The method further includes the step of generating a second clock signal and a third clock signal by dividing down the first clock signal for respectively providing to the microprocessor and converter clock signals of respectively reduced frequency. Additionally, the method includes the steps of converting digital data output from the microprocessor into digital packet data by the converter for output to the transmitter, and transmitting the digital packet data modulated on the first clock signal.

Alternatively, the present method for transmitting data includes the step of generating at a local oscillator a first clock signal at a radio frequency in response to the frequency signal received from the external crystal oscillator upon receipt of a control signal from the microprocessor to start generation of the first clock signal. The method includes the steps of generating a second clock signal using an RC oscillator, and generating a third clock signal from the first clock signal output from the local oscillator for being coupled to the converter. The third clock frequency is a lower frequency than a frequency of the first clock signal. The method further includes the step of generating a fourth clock signal from the second clock signal for coupling to the microprocessor. The fourth clock signal is a lower frequency than the frequency of the first clock signal and is a higher frequency than the third clock signal. Still further, the method includes the steps of outputting digital data from the microprocessor for transmission by the transmitter, converting the digital data output from the microprocessor into digital packet data by the converter, and modulating the digital packet data with the first clock signal received at the transmitter for transmitting an RF signal therefrom.

Rofougaran, et al., the main reference cited by the Examiner, is directed to an adaptive radio transceiver which includes an antenna 8, a switch 9, a receiver 10, a transmitter 12, a local oscillator (LO) generator 14, controller 16, and a self-testing unit 18, as shown in Fig. 1 of the reference. All of these components can be packaged for integration into a single IC. The transmitter 12 modulates

incoming data onto a carrier frequency. The modulated carrier is up converted by the reference signal from the local oscillator generator 14 and amplified to a sufficient power level for radiation into free space through the antenna 8. The controller 16 performs the adaptive programming of the receiver 10, transmitter 14, and the local oscillator generator 16 in addition to adaptive collaboration of the same components of the system. Controller 16 can be controlled externally by a processing device, such as for example, a microprocessor.

Referring to Fig. 2 of the reference, the local oscillator generator 14 provides the infrastructure for frequency planning and includes an intermediate frequency (IF) clock generator 44 and an RF clock generator 47. The IF clock generator includes an oscillator 38 operating at a ratio of the RF signal (fosc). The oscillator 38 may be implemented with the crystal oscillator. The reference frequency output from the oscillator 38 is coupled to a divider 40 which divides the reference signal by a number L to generate the IF clocks for down converting the complex IF signal in the receiver to base band. Clock generator 41 is positioned at the output of the divider 40 to generate a quadrature sinusoidal signal from the square wave output of the diver 40.

It is respectfully submitted that in contrast to the present invention, the frequency signal is generated internally by the crystal oscillator 38, which is positioned <u>inside</u> the integrated circuit. The local oscillator 38 <u>does not</u> receive a frequency signal from an external crystal oscillator to start generation of the clock

signal.

In contradistinction to the arrangement of the Rofougaran, et al., in the present transmitter system, there is an external crystal oscillator 22 positioned externally to the IC 10. The local oscillator, receives the frequency signal from the external crystal oscillator and, responsive thereto, generates a first clock signal having a frequency in a radio frequency band. This feature is completely missing in Rofougaran, et al.

In further contradistinction between the present system and the cited Patent, the Examiner admits that Rofougaran, et al. fails to teach a converter coupled to the microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system. In order to remedy this deficiency of Rofougaran, et al., the Examiner cited a Prockup Patent which is directed to an automatic frequency deviation detection and correction apparatus. The Examiner asserts that the converter 74 shown in Fig. 4 of Prockup constitutes the converter of the present invention, and suggests the combination of the two references, Rofougaran, et al. and Prockup, to result in the transmitter system of the present invention.

It is respectfully submitted, that in contrast to the present invention, the converter 74 in the Prockup Patent, is a D/A converter, e.g., converts digital signals from microprocessor 30 into an analog form (column 4, lines 27-29). It is clear therefore that, although receiving a digital signal at the input thereof, the

converter 74 produces an analog signal at its output, and therefore does not constitute a converter in which digital data output from the microprocessor are converted into digital packet data to be transmitted by the system.

Further, similar to the Rofougaran, et al. reference, in Prockup Patent the crystal oscillator is a local oscillator and does not receive a frequency signal from the external crystal oscillator as it is the case in the present invention.

The Examiner further admits that the combination of Rofougaran, et al. and Prockup fails to teach a clock switch coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter wherein the third clock signal is of a different frequency than the first clock signal and the second clock signal. The clock switch having an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal.

For this purpose the Examiner cites Ishigaki which teaches a clock switch coupled to the local oscillator. Ishigaki is directed to a spread spectrum modulating and demodulating apparatus for transmission and reception of signals. Ishigaki does present a local oscillator which follows the active mode of the switch SW1 under the control of a data processor, and frequency dividers dividing a frequency of an output signal of the local oscillator by predetermined integers. It is respectfully submitted, however, that similar to the previously discussed

Rofougaran, et al. and Prockup, and in contrast to the present system, there is not an external crystal oscillator in Ishigaki which would supply the frequency signal to the local oscillator.

In further contradistinction to the present invention, Ishigaki fails to teach a converter coupled to the data processor for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system.

Tian, a secondary reference, was cited by the Examiner for teaching an RC oscillator for generating the second clock signal - the feature missing from Rofougaran, et al., Prockup and Ishigaki.

Tian is directed to RC oscillator circuits implemented within integrated circuits and switching the integrated oscillator circuit. Similarly to the previously discussed prior art references and in contradistinction with the present invention, Tian fails to employ an external crystal supplying a frequency signal to a local oscillator or generation of a clock signal at the local oscillator responsive to the external crystal frequency signal. Further, Tian fails to teach an RF transmitting system with a microprocessor, or a converter coupled to the microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system, or a clock switch for receiving a command from the microprocessor to start the local oscillator to generate the first clock signal, e.g. the components of the present single crystal oscillator RF transmitter system required for functioning thereof.

Yamazaki, et al., another secondary reference cited by the Examiner, as teaching a peripheral circuit connected to the microprocessor and a resistor network for determining the second clock signal, is directed to low power baud rate generator which has a first oscillator that generates a first clock and a second oscillator that generates a second clock signal with higher frequency. In Yamazaki, et al. as shown in Fig. 1 thereof, the first oscillator 2 is coupled to an external resonator 8 such as a crystal that resonates at a frequency f_1. This enables the first oscillator 2 to generate a first clock signal CLK1 of the frequency f_1. This first clock signal CLK1 is a system clock signal that is supplied to the CPU 4.

The second oscillator 10 is a resistor capacitor RC oscillator. This oscillator 10 oscillates at a higher frequency than the first oscillator 2 and is controlled by an ENABLE signal output by the CPU 4 and oscillates only when ENABLE is active. The output of the second oscillator 10 is a second clock signal CLK2 with a frequency $f_2 > f_2$.

The programmable frequency divider 16 receives two signals from the CPU 4: a division ratio N3 and a LOAD signal. It also receives a second clock signal CLK2 from the second oscillator 10. When the LOAD signal becomes active, the programmable frequency divider 16 loads the value N3 and divides the frequency f_2 of the CLK2 signal by N3 to generate a third clock signal CLK3. The CLK3 signal is provided to the serial port 6 for transmission to other devices.

It is respectfully submitted that in the present system, in contradistinction to

Yamazaki, et al., the clock signal from the local oscillator which is coupled to the external crystal is received at the transmitter. In Yamazaki, et al., however, the clock signal generated at the local oscillator which is coupled to the external crystal is supplied to the CPU, but not to the output serial port. The output port in Yamazaki et al., in contrast to the present arrangement, receives the divided clock signal of the local oscillator which is not connected to the external crystal.

Furthermore, in Yamazaki, et al., in contrast to the present system, the CPU does not control the oscillator 2 which is coupled to the external crystal, but, quite to the contrary, controls the oscillator 10 which is not connected to the external crystal 8.

In the present invention, in further contrast to Yamazaki, et al., the local oscillator generates a first clock signal of a radio frequency responsive to the external crystal oscillator upon receipt of a control signal from the microprocessor to start generation of the clock signal. In Yamazaki, et al. CPU 4 does NOT control the oscillator which is connected to the external crystal oscillator 8 as it is the case in the present invention.

Additionally, in contrast to Yamazaki, et al., the microprocessor in the present system receives a clock signal which is a division of the clock signal generated by the local oscillator connected to the external crystal. In Yamazaki, et al., however, the clock signal, specifically the clock signal CLK3, which is a division of the clock signal generated at the local oscillator 10, is connected not to

the CPU 4 but to the serial port for being transmitted to the peripheral devices. The CPU 4 receives the CLK1 signal from the local oscillator which is connected to the external crystal – quite a different arrangement then in the present system.

Even further, Yamazaki, et al., in contrast to the present invention, fails to teach a converter coupled to the CPU for converting the digital data output from the CPU into digital packet data to be transmitted by the system.

Therefore, none of the references cited by the Examiner, singly or in combination, teach the following claimed recitations of the newly-amended Independent Claims, specifically:

In Claim 1:

"… a converter coupled to said microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system …" or

"… a local oscillator receiving a frequency signal from the external crystal oscillator and generating a first clock signal …responsively to said external crystal oscillator frequency signal…

… providing a second clock signal at a lower frequency than the first clock signal to the microprocessor …" or

"… transmitter … coupled to the local oscillator for use of the first clock signal …";

In Claim 14:

"… generating at … local oscillator a first clock signal … responsive to the external crystal oscillator frequency signal … for providing to the transmitter …" or

"… converting the digital data output from the microprocessor into digital packet data by the converter for output to the transmitter …";

In Claim 16:

"… generating at … local oscillator a first clock signal … responsive to the external crystal oscillator frequency signal …" or

" … converting the digital data output from the microprocessor into digital packet data by the converter; and

modulating the digital packet data with the first clock signal in the transmitter …".

As the Rofougaran, et al., Prockup, Ishigaki, as well as Tian or Yamazaki, et al., solely or in combination, fail to disclose or suggest the concatenation of limitations that define the invention of the subject Patent Application, as now claimed, they cannot make obvious that invention. Therefore newly amended Claims 1, 14 and 16 are believed to be allowable; and the same is respectfully requested.

The Claims respectively dependent on Claims 1, 14, and 16 are believed to add further patentably distinct limitations, but are at least patentably distinct for the same reasons as the independent claim upon which they are dependent.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

If there are any further charges associated with this filing, the Honorable Commissioner for Patents is hereby authorized to charge Deposit Account #18-2011 for such charges.

Respectfully submitted,
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